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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/873,580	06/04/01	FUJITA H	P/2171-196

002352 MMC2/1012
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EXAMINER	
TOLEDO, F	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/12/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/873,580	FUJITA, HARUMITSU	
	Examiner	Art Unit	
	Fernando Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 12/26/97. It is noted, however, that applicant has not filed a certified copy of the Japanese application as required by 35 U.S.C. 119(b).

Information Disclosure Statement

2. The information disclosure statement filed 6/04/01 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tigelaar et al. (U. S. patent 5,595,922) in view of Wolf "Silicon Processing for the VLSI Era Volume 2: Process Integration (pp. 354 – 361)."

In re claim 1; Tigelaar in the U. S. patent 5,595,922; figures 1 – 5 and related text, shows preparing a semiconductor substrate having several active regions of a first conductivity type (column 2); forming first gate oxide films 18 onto the several active

regions (figure 1); forming an electrode layer 20 on the first gate oxide films (figure 1); pattering the electrode layer to form gate electrode patterns onto each of the several active regions (figure 2); oxidizing the surface of the gate electrode patterns to from a second gate oxide film which is integrated with the first oxide film and gradually decreases in thickness from side walls of the gate electrode pattern towards a center portion thereof (figure 4).

Tigelaar does not show first doping the several active regions at first concentrations with an impurity of a second conductivity type which is opposite to the first conductivity type using the gate electrode as a pattern mask, to dope the gate electrode patterns and the active region on either side thereof at low concentration and second doping while covering a portion of the plurality of active regions by a mask, reminder of the active regions at second concentration higher than the first concentration with an impurity of a second conductivity type, to dope the gate electrode patterns and the active regions on either side thereof at a second concentration in the reminder of the active regions.

However, Wolf in the textbook "Silicon Processing for the VLSI Era Volume 2: Process Integration; pp 354 – 361 and related figures, teaches that it is conventional to have drain structures in MOS devices and that the use of LDD's is to absorb some of the potential into the drain and reduce the maximum electric field (E_M) (page 354).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to dope a first time to form the LDD's in the invention of Tigelaar because as shown by Wolf the LDD's will help absorb some of the potential

into the drain and reduce the E_M, and also to dope a second time in order to form a source and drain as it is conventional absent to evidence to the contrary.

In re claim 2; Wolf teaches that the doping steps to form the LDD's and source and drain are done by ion implanting (page 354 – 355).

In re claim 3; Wolf teaches forming spacers of insulating material on side walls of the gate electrode patterns between the first doping step and the second doping step (page 354).

In re claim 4; Tigelaar teaches wherein the several of MOS transistors includes MOS transistors driven at first voltage and MOS transistors driven at a second voltage which is higher than the first voltage (column 2).

In re claim 5; Tigelaar teaches that the first oxide films forms gate oxide films of the MOS transistor at the second voltage and the MOS transistors driven at the first voltage commonly in same processing step (figure 1).

In re claim 6; Tigelaar teaches wherein the gate electrode patterns of MOS transistor driven at the second voltage are doped at a first concentration and the gate electrode patterns of MOS transistors driven at the relatively low voltage are doped at a second concentration (column 2).

In re claim 7; Tigelaar teaches wherein the semiconductor substrate comprises several active regions of a second conductivity type, and the step of forming the first gate oxide films, the step of forming the electrode layers, the step of forming the electrode patterns, the step of forming the second gate oxide films are carried out commonly for the plurality of active regions of a second conductivity type (figures 1 – 4).

In re claim 8; Wolf teaches ion implanting an impurity of a first conductivity type at a low concentration commonly in the plurality of active regions of a second conductivity type; and ion implanting an impurity of a first conductivity type at high concentration in a portion of several active regions of a second conductivity type (figure 5-33, page 359).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando Toledo whose telephone number is (703) 305-0567. The examiner can normally be reached on Monday – Friday, 8am – 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

	Fernando Toledo Patent Examiner Art Unit 2823

ft
October 9, 2001

Carl Whitehead Jr.
CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800